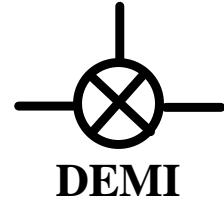


Design Note



To: Owners of all Transverter Models 903-144 and 1296-144 with a 5 volt regulator in the VR3 position
From: DEMI R&D Dept.
DN#: 005 - Parts kit # DN005K
Date: August 15, 2002
Re: IP3 improvement for 903 and 1296 MHz. transverters

Performance Improvement

When originally designed, the 903 and 1296 MHz. transverter models had their bias points of the GaAs FET preamplifier adjusted for best noise figure. After some further engineering from our R&D department, it has been discovered that the -1dB compression point can be improved by 3 dB or more which will result in a IP3 improvement of over 6 dB for the LNA. This improvement can be achieved with little or no degradation to the transverters system noise figure. The reason for this modification is to deter front end compression caused by strong out of band signals.

Circuit Change Description

The GaAs FET's in the 903 and 1296 transverters were originally biased for approximately 20 - 25 mA current with 2.0 - 2.5 Volts on the drain. This was derived from a 5 volt regulated supply and a 150 ohm voltage dropping resistor. The source resistors were adjusted up or down from 50 ohms to produce the desired results. To improve the IP3, the FET should be biased at 55-65 mA., maintaining the 3.0 volts on the drain. To simply replace the 150 ohm drain resistor with 33 ohm would load the circuit down too much. Placing a RF choke in the drain voltage supply would cause a potential instability. Some resistor loading is required on the output of the FET to provide broad band matching and stability. It then becomes necessary to change the regulated voltage to 9 volts and replace the 150 resistor with a 100 ohm. ½ watt resistor. (loading and stability) Because of the current drain, a ¼ version would be over dissipated. (.360 mW @ 60mA) A starting point for source resistors should be around 12 ohms (2 - 24 ohms chips, 1 one each source lead) The total source resistance should be between 8 and 15 ohms depending on the FET. Set the bias and retune the 2 input capacitors as before for gain and noise figure. In some cases, the shunt inductor value may need to be increased to achieve best performance.

Caution!

Be sure that the source resistors are in place before applying any voltage that exceeds 5 volts to the Drain of any FET. In this design, the Gate is at DC ground potential and the delta of greater than 5 volts (Gate to Drain) will cause permanent damage to the FET. Measure source to ground resistance with a ohm meter before applying voltage.

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